GP-448-3 (NP-1480)

(7)

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-263268
(43)Date of publication of application : 13.10.1995

(51)Int.Cl. H01F 41/04
H05K 1/14

(21)Application number : 06-046620
(22)Date of filing : 17.03.1994

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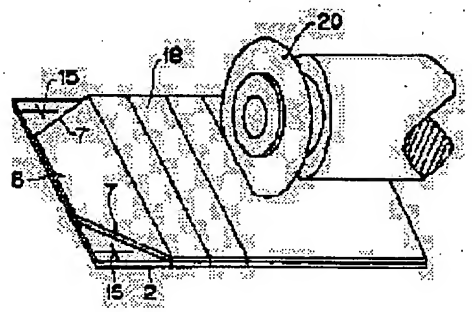
(54) MANUFACTURE OF ELECTRONIC COMPONENT

(57)Abstract:
PURPOSE: To align and bond substrates to each other with good accuracy and at low production costs even without using a high-cost apparatus and to cut out an electronic-component chip with good accuracy from an electronic- component aggregate substrate.
CONSTITUTION: An insulator substrate 2 in which a conductor for a coil and alignment marks 15 have been formed on the same face is bonded to an insulator substrate 6 in which cutouts 7 used to expose the alignment marks 15 have been formed, and an inductor aggregate substrate 18 is constituted. The conductor for the coil and the alignment marks 15 are set so as to have a prescribed positional relationship. While the alignment marks 15 exposed from the cutouts 7 are used as criterions, the aggregate substrate 18 is cut by using a cutting whetstone 20 for a cutting apparatus, and chips are cut out.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

JAPANESE [JP,07-263268,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD EFFECT OF THE INVENTION TECHNICAL PROBLEM OPERATION EXAMPLE DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

CLAIMS

[Claim(s)]
[Claim 1] the whole surface of the 1st substrate — a pattern — a conductor and this pattern — the process which prepares the alignment mark which has position relation to a conductor, and said alignment mark — exposing — and said pattern — so that a conductor may be inserted The manufacture approach of the electronic parts characterized by having the process which joins said 1st substrate and 2nd substrate and constitutes an electronic-parts aggregate substrate, and the process which cuts down the electronic-parts chip of predetermined size from said electronic-parts aggregate substrate on the basis of said exposed alignment mark.
[Claim 2] The process which prepares a conductor and this 1st alignment mark that has position relation to a conductor the 1st pattern the 1st pattern in the whole surface of the 1st substrate, The process which prepares a conductor and this 2nd alignment mark that has position relation to a conductor the 2nd pattern the 2nd pattern in the whole surface of the 2nd substrate, and where [said] the 2nd alignment mark is carried out to a conductor outside the 2nd pattern said 1st alignment mark — exposing — and — said — so that a conductor may be inserted the 1st pattern The process which considers alignment between the 2nd substrate as said 1st substrate on the basis of said 1st alignment mark and said 2nd alignment mark after piling up said 1st substrate and 2nd substrate, The manufacture approach of the electronic parts characterized by having the process which joins said 2nd substrate to said 1st substrate, and constitutes an electronic-parts aggregate substrate, and the process which cuts down the electronic-parts chip of predetermined size from said electronic-parts aggregate substrate.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention — the interior — a pattern — it is related with the manufacture approach of electronic parts equipped with the conductor.
[0002]
[Description of the Prior Art] In the manufacture approach of the electronic parts constituted by joining two or more substrates, the approach of carrying out alignment between substrates on the basis of the substrate edge conventionally, and joining was learned. Moreover, how to cut down the electronic-parts chip of predetermined size from an electronic-parts aggregate substrate on the basis of the substrate edge was also learned. However, since it was difficult for these approaches to finish the substrate edge with high precision, they had the problem that alignment precision and logging precision were low.
[0003] Moreover, as an option, an alignment mark is prepared in a substrate and there is a method of performing alignment between substrates on the basis of this alignment mark. Moreover, there is also the approach of cutting down the electronic-parts chip of predetermined size from an electronic-parts aggregate substrate on the basis of an alignment mark. These approaches need to prepare an alignment mark in fields other than a plane of composition, although precision becomes high rather than the approach on the basis of the substrate edge. It is because an alignment mark is put between a substrate, and disappears and it becomes impossible to use as criteria if an alignment mark is prepared in a plane of composition, after joining a substrate. therefore, when a manufacture man day increases or the alignment mark is prepared in the front flesh side of a substrate, expensive double-sided alignment equipment is extraordinarily required — etc. — a problem newly occurs.
[0004] Then, even if expensive equipment is not used for the technical problem of this invention, with a cheap manufacturing cost, precision can improve both substrates alignment, and it can be joined, and is to offer the manufacture approach of the electronic parts which can cut down an electronic-parts chip with a sufficient precision from an electronic-parts aggregate substrate.
[0005]
[Means for Solving the Problem and its Function] In order to solve the above technical problem, the manufacture approach of the electronic parts concerning this invention (a) — the whole surface of the 1st substrate — a pattern — a conductor and this pattern — the process which prepares the alignment mark which has position relation to a conductor, and (b) — said alignment mark — exposing — and said pattern — so that a conductor may be inserted Said 1st substrate and 2nd substrate are joined and it is characterized by having the process which constitutes an electronic-parts aggregate substrate, and the process which cuts down the electronic-parts chip of predetermined size from said electronic-parts aggregate substrate on the basis of said alignment mark which carried out (c) exposure.
[0006] In the above approach, since the alignment mark prepared in the 1st substrate is exposed, it becomes unnecessary to prepare an alignment mark in any fields other than a plane of composition like before, and a manufacture man day decreases. And since logging of the electronic-parts chip from an electronic-parts aggregate substrate is performed on the basis of an alignment mark, logging precision becomes high.
[0007] Moreover, the process at which the manufacture approach of the electronic parts concerning this invention prepares a conductor and this 1st alignment mark that has position relation to a conductor the 1st pattern the 1st pattern in the whole surface of the (d) 1st substrate, (e) — the process which prepares a conductor and this 2nd alignment mark that has position relation to a conductor the 2nd pattern the 2nd pattern in the whole surface of the 2nd substrate, and (f), where [said] the 2nd alignment mark is carried out to a conductor outside the 2nd pattern said 1st alignment mark — exposing — and — said — so that a conductor may be inserted the 1st pattern The process which considers alignment between the 2nd substrate as said 1st substrate on the basis of said 1st alignment mark and said 2nd alignment mark after piling up said 1st substrate and 2nd substrate, (g) It is characterized by having the process which joins said 2nd substrate to said 1st substrate, and constitutes an electronic-parts aggregate substrate, and the process which cuts down the electronic-parts chip of predetermined size from the (h) aforementioned electronic-parts aggregate substrate.
[0008] In the above approach, since the 1st alignment mark and the 2nd alignment mark can be seen from the same, alignment of the 1st substrate and the 2nd substrate is performed with a sufficient precision using cheap one side alignment equipment.
[0009]

[Example] Hereafter, the example of the manufacture approach of the electronic parts concerning this invention is explained with reference to an accompanying drawing.
The 1st example of [the 1st example, drawing 1 - drawing 9] explains the manufacture approach of an inductor 1 shown in drawing 1 .
[0010] an inductor 1 — the object for coils — the insulator substrate 2 which formed the conductor 3 in the top face, and the insulator substrate 6 which nothing forms in a front face are joined with adhesives 8. As an ingredient of substrates 2 and 6, a ferrite etc. is used, for example. a substrate 2 is shown in drawing 2 — as — a top face — an insulator layer (for example, polyimide film) 4 — minding — the object for spiral coils — the conductor 3 is formed. the object for coils — one edge 3a of a conductor 3 is exposed to the right-hand side edge of a substrate 2, and other-end section 3b is taken about from the center section of a substrate 2 through through hole 3c prepared in the insulator layer 4 at the left-hand side edge.
[0011] The external electrodes 10 and 11 are formed in the edge of right and left of an inductor 1, respectively. the object for coils — edge 3b of a conductor 3 is electrically connected to the external electrode 10, and edge 3a is electrically connected to the external electrode 11. Next, the manufacture procedure of the inductor 1 which has the above structure is explained. Usually, in the mass production of a chip, it is manufactured in the state of the aggregate substrate containing two or more chips. an inductor 1 is similarly shown in drawing 3 and drawing 4 — as — the object for the coils of plurality [substrate / 2] — the alignment mark 15 for regulating the mutual physical relationship of conductors 3, those conductors, and an insulating-layer pattern is formed. namely, the top face of a substrate 2 — first — the whole surface — a means besides vacuum evaporationo, sputtering, and plating — a conductor — the film is formed. Next, after applying a photosensitive resist, a predetermined pattern can be burned with an exposure machine, and if negatives are developed, the photosensitive resist of an unnecessary part will be removed. next, the conductor exposed from the photosensitive resist — after etching a film part, all photosensitive resists exfoliate. in this way, the object for coils — the pattern of the conductor equivalent to edge 3b of a conductor 3 and the pattern of the alignment mark 15 is formed. Next, the polyimide resin of for example, ultraviolet-rays hardenability or its precursor is applied all over a substrate, and the insulator layer which left the formation part of edge 3b by exposure, development, and hardening is formed. The suitable alignment mark for a photo mask can be installed in pattern doubling at this time, and it can be made to agree with the alignment mark 15. next, the same pattern formation means — the object for spiral-like coils — formation of edge 3a is considered as a conductor 3. The alignment mark 15 can be used also for the alignment at this time. In addition, the pattern formation of a conductor and an insulator layer may not be based on said thin film method of construction, but may be based on a thick-film method of construction besides selection plating or screen-stencil.
[0012] the alignment mark 15 is formed in at least two corners of the near side of a substrate 2 — having — the object for coils — a conductor 3 aligns in all directions into the part surrounded with the alternate long and short dash line 17, and is arranged. and the alignment mark 15 — these objects for coils — it has position relation to the conductor 3. the substrate 6 which nothing forms in a front face at this substrate 2 — adhesives 8 — minding — joining — a substrate 2 and a substrate 6 — the object for coils — a conductor 3 is put. The notch 7 is formed in two corners of the near side of a substrate 6, and the alignment mark 15 has exposed after junction of a substrate 2 and a substrate 6 from the notch 7 (refer to drawing 5). In this way, the inductor aggregate substrate 18 which consists of a substrate 2 and a substrate 6 is obtained.
[0013] Next, after setting the aggregate substrate 18 to the processing table of cutting equipment, the location of a processing table is adjusted detecting looking at the alignment mark 15, as shown in drawing 6 , the alignment mark 15 is started, and it is made to move to a criteria location. Then, as shown in drawing 7 , the aggregate substrate 18 is cut in all directions at the predetermined spacing on the basis of the alignment mark 15 by the cutting off wheel 20 of cutting equipment. In this way, the chip 22 cut into predetermined size is obtained (refer to drawing 8 and drawing 9). The external electrodes 10 and 11 are formed in the both ends of the obtained chip 22 by approaches, such as vacuum evaporationo and sputtering, or plating, spreading of conductive paste, etc., and it considers as the inductor 1 shown in drawing 1 .
[0014] In the manufacture approach of the above inductor 1, since the alignment mark 15 was exposed from the notch 7, the logging location of each chip 22 can be decided with a sufficient precision on the basis of this alignment mark 15. Therefore, a chip 22 can be cut down with a sufficient precision. moreover, the alignment mark 15 — the plane of composition for coils of a substrate 2, i.e., an object, — since what is necessary is just to prepare in the field in which the conductor 3 is formed, it becomes unnecessary to prepare an alignment mark to fields other than a plane of composition (for it to be the inferior surface of tongue of a substrate 2 in the case of this example) specially like before Consequently, the pattern formation process of substrate 2 inferior surface of tongue can be skipped, cheap double-sided alignment equipment also becomes unnecessary, and a manufacturing cost can be lowered.
[0015] The 2nd example of [the 2nd example, drawing 10 - drawing 16] explains the manufacture approach of an inductor 31 shown in drawing 10 . an inductor 31 — the object for coils — a conductor 33, the insulator substrate 32 which formed the screening electrode 34 in the vertical side, respectively, and the insulator substrate 36 which formed the screening electrode 37 in the top face are joined with adhesives 38.
[0016] the insulator substrate 32 — a top face — an insulator layer (for example, polyimide film) 35 — minding — the object for spiral coils — the conductor 33 is formed. the object for coils — one edge 33a of a conductor 33 is electrically connected to the external electrode 41 prepared in the right end section of an inductor 31. the object for coils — other-end section 33b of a conductor 33 is taken about on left-hand side from the center section of the

inductor 31 through through hole 33c prepared in the insulator layer 35, and is electrically connected to the external electrode 40 prepared in the left end section of an inductor 31.

[0017] Next, the manufacture procedure of the inductor 31 which has the above structure is explained. it is shown in drawing 11 and drawing 12 — as — the object for the coils of the plurality [substrate / 32] in the means of for example, photograph RISOGURAFU — a conductor 33 and a screening electrode 34, and two alignment marks 43 or more are formed. namely, the vertical side of a substrate 32 — a means besides vacuum evaporationo, sputtering, and plating — a conductor — the film is formed. Next, a substrate 32 is set to a double-sided exposure machine after applying a photosensitive resist all over the upper and lower sides of a substrate 32. At this time, a substrate 32 is put between the photo masks of two sheets made to correspond to 1 to 1. And after exposing the vertical side of a substrate 32 to coincidence, a photosensitive resist is developed and the photosensitive resist of an unnecessary part is removed. Next, after etching the thin film part exposed from the photosensitive resist, all the photosensitive resists that remain are removed. in this way, the object for coils — edge 33b, the alignment mark 43, and screening electrode 34 of a conductor 33 are formed.

[0018] Next, all over a substrate 32, the polyimide resin of ultraviolet-rays hardenability or its precursor is applied, and the insulator layer 35 which left the formation part of edge 33b by exposure, development, and hardening is formed. The suitable alignment mark for a photo mask can be installed in pattern doubling at this time, and it can be made to agree with the alignment mark 43. next, the whole top-face surface of a substrate 32 — a means besides vacuum evaporationo, sputtering, and plating — a conductor — the film is formed. Next, after applying a photosensitive resist, a predetermined pattern can be burned with an exposure machine, and if negatives are developed, the photosensitive resist of an unnecessary part will be removed. next, the conductor exposed from the photosensitive resist — after etching a film part, all photosensitive resists exfoliate. in this way, the object for spiral-like coils — a conductor 33 and edge 33a are formed. The alignment mark 43 can be used also for the alignment at this time.

[0019] in this example, the alignment mark 43 is formed in two corners of the near side of a substrate 32 — having — the object for coils — a conductor 33 and the screening electrode 34 which has countered this align in all directions into each part surrounded with the alternate long and short dash line 45, and is arranged. and the alignment mark 43 — these objects for coils — it has position relation to the conductor 33 and the screening electrode 34.

[0020] On the other hand, the substrate 36 is also formed for the same for example, two or more screening-electrodes [with the means of photograph RISOGURAFU] 37, and two alignment mark 44 in the top face. The alignment mark 44 is formed in two corners by the side of the back of a substrate 36, and a screening electrode 37 aligns in all directions into each part surrounded with the alternate long and short dash line 46, and is arranged. And the alignment mark 44 has position relation to these screening electrodes 37. Furthermore, the notch 47 is formed in two corners of the near side of a substrate 36.

[0021] next, the substrate 32 — adhesives 8 — minding — a substrate 36 — joining — the object for coils — a conductor 33 is put. A substrate 32 and alignment between 36 are performed on the basis of the alignment marks 43 and 44, detecting, looking at the alignment marks 43 and 44 using one side alignment equipment 50, since the alignment mark 43 is exposed from the notch 47 at this time as shown in drawing 13 . In this way, as shown in drawing 14 , the inductor aggregate substrate 48 which consists of substrates 32 and 36 is obtained.

[0022] Next, looking at the alignment mark 43 (or 44), after setting the aggregate substrate 48 to the processing table of cutting equipment, the location of a processing table is adjusted detecting, the alignment mark 43 (or 44) is started, and it is made to move to a criteria location. Then, the aggregate substrate 48 is cut in all directions at the predetermined spacing on the basis of the alignment mark 43 (or 44) in cutting off wheel of cutting equipment (drawing 15 and 16 reference). In this way, the chip 49 cut into predetermined size is obtained. The external electrodes 40 and 41 are formed in the both ends of the obtained chip 49 by approaches, such as vacuum evaporationo and sputtering, or plating, spreading of conductive paste, etc., and it considers as the inductor 31 shown in drawing 10 .

[0023] In the manufacture approach of the above inductor 31, since the alignment mark 43 prepared in the substrate 32 was exposed from the notch 47, precision is improved by the alignment of substrates 32 and 36 on the basis of this alignment mark 43 and the alignment mark 44 prepared in the substrate 36. Therefore, precision is improved by junction of substrates 32 and 36. Moreover, alignment of substrates 32 and 36 can be carried out using cheap one side alignment equipment, without being able to see the alignment marks 43 and 44 from the same, and using expensive double-sided alignment equipment. Furthermore, each chip 49 can be cut down with a sufficient precision on the basis of these alignment marks 43 and 44.

[0024] the manufacture approach of the electronic parts concerning example] this invention besides [is not limited to said example, within the limits of the summary, can be boiled variously and can deform. although the notch was prepared in said example in order to expose an alignment mark — also ******(ing) — it is not necessary to prepare a notch and to also restrict the number of alignment marks to two pieces for example, the insulator substrate 55 which formed holes 56 and 57 as shown in drawing 17 — a circuit — it joins to a conductor and the insulator substrate 54 which prepared the alignment mark, and you may make it exposed [an alignment mark] from holes 56 and 57 moreover, it is shown in drawing 18 — as — the circular insulator substrate 61 — a circuit — it joins to a conductor and the insulator substrate 60 which formed the alignment marks 62 and 63, and you may make it exposed [the alignment marks 62 and 63] moreover, it is shown in drawing 19 — as — the rectangle insulator substrate 66 — a circuit — it joins to a conductor and the insulator substrate 65 which formed four alignment

marks 67, 68, 69, and 70, and you may make it exposed [the alignment marks 67-70]
[0025] furthermore, an alignment mark — said example — like — a circuit — a conductor — a coincidence term — you may form — a circuit — a conductor — with the time of formation, you may form independently at another stage. however, a circuit — if a conductor and an alignment mark are formed at a coincidence term, while alignment precision and logging precision will improve more, a manufacture man day also decreases. moreover, a circuit — a conductor — the object for coils — without restricting to a conductor, if it has an electric function, a configuration, the quality of the material, etc. will not be asked.
[0026]
[Effect of the Invention] By the above explanation, since the alignment mark prepared in the 1st substrate is exposed according to this invention so that clearly, the electronic-parts chip from an electronic-parts aggregate substrate can be cut down with a sufficient precision on the basis of this alignment mark. moreover, an alignment mark — a pattern — since what is necessary is just to prepare in the same field as a conductor, it becomes unnecessary to prepare an alignment mark in any fields other than a plane of composition like before, and a manufacture man day can be lessened.
[0027] Moreover, since the 1st alignment mark prepared in the 1st substrate is exposed, precision is improved by the alignment of the 1st substrate and the 2nd substrate on the basis of the 1st alignment mark and the 2nd alignment mark. Furthermore, alignment of the 1st substrate and the 2nd substrate can be carried out using cheap one side alignment equipment, without using expensive double-sided alignment equipment, since the 1st alignment mark and the 2nd alignment mark can be seen from the same.
[0028] Consequently, even if it does not use expensive equipment, with a cheap manufacturing cost, precision can improve both substrates alignment, it can join, and an electronic-parts chip can be cut down with a sufficient precision from an electronic-parts aggregate substrate.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Industrial Application] this invention — the interior — a pattern — it is related with the manufacture approach of electronic parts equipped with the conductor.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] By the above explanation, since the alignment mark prepared in the 1st substrate is exposed according to this invention so that clearly, the electronic-parts chip from an electronic-parts aggregate substrate can be cut down with a sufficient precision on the basis of this alignment mark. moreover, an alignment mark — a pattern — since what is necessary is just to prepare in the same field as a conductor, it becomes unnecessary to prepare an alignment mark in any fields other than a plane of composition like before, and a manufacture man day can be lessened.
[0027] Moreover, since the 1st alignment mark prepared in the 1st substrate is exposed, precision is improved by the alignment of the 1st substrate and the 2nd substrate on the basis of the 1st alignment mark and the 2nd alignment mark. Furthermore, alignment of the 1st substrate and the 2nd substrate can be carried out using cheap one side alignment equipment, without using expensive double-sided alignment equipment, since the 1st alignment mark and the 2nd alignment mark can be seen from the same.
[0028] Consequently, even if it does not use expensive equipment, with a cheap manufacturing cost, precision can improve both substrates alignment, it can join, and an electronic-parts chip can be cut down with a sufficient precision from an electronic-parts aggregate substrate.

[Translation done.]

* NOTICES *

TECHNICAL PROBLEM

[Description of the Prior Art] In the manufacture approach of the electronic parts constituted by joining two or more substrates, the approach of carrying out alignment between substrates on the basis of the substrate edge conventionally, and joining was learned. Moreover, how to cut down the electronic-parts chip of predetermined size from an electronic-parts aggregate substrate on the basis of the substrate edge was also learned. However, since it was difficult for these approaches to finish the substrate edge with high precision, they had the problem that alignment precision and logging precision were low.

[0003] Moreover, as an option, an alignment mark is prepared in a substrate and there is a method of performing alignment between substrates on the basis of this alignment mark. Moreover, there is also the approach of cutting down the electronic-parts chip of predetermined size from an electronic-parts aggregate substrate on the basis of an alignment mark. These approaches need to prepare an alignment mark in fields other than a plane of composition, although precision becomes high rather than the approach on the basis of the substrate edge. It is because an alignment mark is put between a substrate, and disappears and it becomes impossible to use as criteria if an alignment mark is prepared in a plane of composition, after joining a substrate. therefore, when a manufacture man day increases or the alignment mark is prepared in the front flesh side of a substrate, expensive double-sided alignment equipment is extraordinarily required — etc. — a problem newly occurs.

[0004] Then, even if expensive equipment is not used for the technical problem of this invention, with a cheap manufacturing cost, precision can improve both substrates alignment, and it can be joined, and is to offer the manufacture approach of the electronic parts which can cut down an electronic-parts chip with a sufficient precision from an electronic-parts aggregate substrate.

[Translation done.]

OPERATION

[Means for Solving the Problem and its Function] The manufacture approach of the electronic parts built over this invention in order to solve the above technical problem, (a) the whole surface of the 1st substrate — a pattern — a conductor and this pattern — the process which prepares the alignment mark which has position relation to a conductor, and (b) — said alignment mark — exposing — and said pattern — so that a conductor may be inserted Said 1st substrate and 2nd substrate are joined and it is characterized by having the process which constitutes an electronic-parts aggregate substrate, and the process which cuts down the electronic-parts chip of predetermined size from said electronic-parts aggregate substrate on the basis of said alignment mark which carried out (c) exposure.

[0006] In the above approach, since the alignment mark prepared in the 1st substrate is exposed, it becomes unnecessary to prepare an alignment mark in any fields other than a plane of composition like before, and a manufacture man day decreases. And since logging of the electronic-parts chip from an electronic-parts aggregate substrate is performed on the basis of an alignment mark, logging precision becomes high.

[0007] Moreover, the manufacture approach of the electronic parts concerning this invention is on the whole surface of the (d) 1st substrate, The process which prepares a conductor and this 1st alignment mark that has position relation to a conductor the 1st pattern the 1st pattern, (e) — the process which prepares a conductor and this 2nd alignment mark that has position relation to a conductor the 2nd pattern the 2nd pattern in the whole surface of the 2nd substrate, and (f), where [said] the 2nd alignment mark is carried out to a conductor outside the 2nd pattern said 1st alignment mark — exposing — and — said — so that a conductor may be inserted the 1st pattern The process which considers alignment between the 2nd substrate as said 1st substrate on the basis of said 1st alignment mark and said 2nd alignment mark after piling up said 1st substrate and 2nd substrate, (g) It is characterized by having the process which joins said 2nd substrate to said 1st substrate, and constitutes an electronic-parts aggregate substrate, and the process which cuts down the electronic-parts chip of predetermined size from the (h) aforementioned electronic-parts aggregate substrate.

[0008] In the above approach, since the 1st alignment mark and the 2nd alignment mark can be seen from the same, alignment of the 1st substrate and the 2nd substrate is performed with a sufficient precision using cheap one side alignment equipment.

[0009]

[Translation done.]

EXAMPLE

[Example] Hereafter, the example of the manufacture approach of the electronic parts concerning this invention is explained with reference to an accompanying drawing.
The 1st example of [the 1st example, drawing 1 - drawing 9] explains the manufacture approach of an inductor 1 shown in drawing 1 .
[0010] an inductor 1 — the object for coils — the insulator substrate 2 which formed the conductor 3 in the top face, and the insulator substrate 6 which nothing forms in a front face are joined with adhesives 8. As an ingredient of substrates 2 and 6, a ferrite etc. is used, for example. a substrate 2 is shown in drawing 2 — as — a top face — an insulator layer (for example, polyimide film) 4 — minding — the object for spiral coils — the conductor 3 is formed. the object for coils — one edge 3a of a conductor 3 is exposed to the right-hand side edge of a substrate 2, and other-end section 3b is taken about from the center section of a substrate 2 through through hole 3c prepared in the insulator layer 4 at the left-hand side edge.
[0011] The external electrodes 10 and 11 are formed in the edge of right and left of an inductor 1, respectively. the object for coils — edge 3b of a conductor 3 is electrically connected to the external electrode 10, and edge 3a is electrically connected to the external electrode 11. Next, the manufacture procedure of the inductor 1 which has the above structure is explained. Usually, in the mass production of a chip, it is manufactured in the state of the aggregate substrate containing two or more chips. an inductor 1 is similarly shown in drawing 3 and drawing 4 — as — the object for the coils of plurality [substrate / 2] — the alignment mark 15 for regulating the mutual physical relationship of conductors 3, those conductors, and an insulating-layer pattern is formed. namely, the top face of a substrate 2 — first — the whole surface — a means besides vacuum evaporationo, sputtering, and plating — a conductor — the film is formed. Next, after applying a photosensitive resist, a predetermined pattern can be burned with an exposure machine, and if negatives are developed, the photosensitive resist of an unnecessary part will be removed. next, the conductor exposed from the photosensitive resist — after etching a film part, all photosensitive resists exfoliate. in this way, the object for coils — the pattern of the conductor equivalent to edge 3b of a conductor 3 and the pattern of the alignment mark 15 is formed. Next, the polyimide resin of for example, ultraviolet-rays hardenability or its precursor is applied all over a substrate, and the insulator layer which left the formation part of edge 3b by exposure, development, and hardening is formed. The suitable alignment mark for a photo mask can be installed in pattern doubling at this time, and it can be made to agree with the alignment mark 15. next, the same pattern formation means — the object for spiral-like coils — formation of edge 3a is considered as a conductor 3. The alignment mark 15 can be used also for the alignment at this time. In addition, the pattern formation of a conductor and an insulator layer may not be based on said thin film method of construction, but may be based on a thick-film method of construction besides selection plating or screen-stencil.
[0012] the alignment mark 15 is formed in at least two corners of the near side of a substrate 2 — having — the object for coils — a conductor 3 aligns in all directions into the part surrounded with the alternate long and short dash line 17, and is arranged. and the alignment mark 15 — these objects for coils — it has position relation to the conductor 3. the substrate 6 which nothing forms in a front face at this substrate 2 — adhesives 8 — minding — joining — a substrate 2 and a substrate 6 — the object for coils — a conductor 3 is put. The notch 7 is formed in two corners of the near side of a substrate 6, and the alignment mark 15 has exposed after junction of a substrate 2 and a substrate 6 from the notch 7 (refer to drawing 5). In this way, the inductor aggregate substrate 18 which consists of a substrate 2 and a substrate 6 is obtained.
[0013] Next, after setting the aggregate substrate 18 to the processing table of cutting equipment, the location of a processing table is adjusted detecting looking at the alignment mark 15, as shown in drawing 6 , the alignment mark 15 is started, and it is made to move to a criteria location. Then, as shown in drawing 7 , the aggregate substrate 18 is cut in all directions at the predetermined spacing on the basis of the alignment mark 15 by the cutting off wheel 20 of cutting equipment. In this way, the chip 22 cut into predetermined size is obtained (refer to drawing 8 and drawing 9). The external electrodes 10 and 11 are formed in the both ends of the obtained chip 22 by approaches, such as vacuum evaporationo and sputtering, or plating, spreading of conductive paste, etc., and it considers as the inductor 1 shown in drawing 1 .
[0014] In the manufacture approach of the above inductor 1, since the alignment mark 15 was exposed from the notch 7, the logging location of each chip 22 can be decided with a sufficient precision on the basis of this alignment mark 15. Therefore, a chip 22 can be cut down with a sufficient precision. moreover, the alignment mark 15 — the plane of composition for coils of a substrate 2, i.e., an object, — since what is necessary is just to prepare in the field in which the conductor 3 is formed, it becomes unnecessary to prepare an alignment mark to fields other than

a plane of composition (for it to be the inferior surface of tongue of a substrate 2 in the case of this example) specially like before Consequently, the pattern formation process of substrate 2 inferior surface of tongue can be skipped, cheap double-sided alignment equipment also becomes unnecessary, and a manufacturing cost can be lowered.

[0015] The 2nd example of [the 2nd example, drawing 10 - drawing 16] explains the manufacture approach of an inductor 31 shown in drawing 10 . an inductor 31 — the object for coils — a conductor 33, the insulator substrate 32 which formed the screening electrode 34 in the vertical side, respectively, and the insulator substrate 36 which formed the screening electrode 37 in the top face are joined with adhesives 38.

[0016] the insulator substrate 32 — a top face — an insulator layer (for example, polyimide film) 35 — minding — the object for spiral coils — the conductor 33 is formed. the object for coils — one edge 33a of a conductor 33 is electrically connected to the external electrode 41 prepared in the right end section of an inductor 31. the object for coils — other-end section 33b of a conductor 33 is taken about on left-hand side from the center section of the inductor 31 through through hole 33c prepared in the insulator layer 35, and is electrically connected to the external electrode 40 prepared in the left end section of an inductor 31.

[0017] Next, the manufacture procedure of the inductor 31 which has the above structure is explained. it is shown in drawing 11 and drawing 12 — as — the object for the coils of the plurality [substrate / 32] in the means of for example, photograph RISOGURAFU — a conductor 33 and a screening electrode 34, and two alignment marks 43 or more are formed. namely, the vertical side of a substrate 32 — a means besides vacuum evaporationo, sputtering, and plating — a conductor — the film is formed. Next, a substrate 32 is set to a double-sided exposure machine after applying a photosensitive resist all over the upper and lower sides of a substrate 32. At this time, a substrate 32 is put between the photo masks of two sheets made to correspond to 1 to 1. And after exposing the vertical side of a substrate 32 to coincidence, a photosensitive resist is developed and the photosensitive resist of an unnecessary part is removed. Next, after etching the thin film part exposed from the photosensitive resist, all the photosensitive resists that remain are removed. in this way, the object for coils — edge 33b, the alignment mark 43, and screening electrode 34 of a conductor 33 are formed.

[0018] Next, all over a substrate 32, the polyimide resin of ultraviolet-rays hardenability or its precursor is applied, and the insulator layer 35 which left the formation part of edge 33b by exposure, development, and hardening is formed. The suitable alignment mark for a photo mask can be installed in pattern doubling at this time, and it can be made to agree with the alignment mark 43. next, the whole top-face surface of a substrate 32 — a means besides vacuum evaporationo, sputtering, and plating — a conductor — the film is formed. Next, after applying a photosensitive resist, a predetermined pattern can be burned with an exposure machine, and if negatives are developed, the photosensitive resist of an unnecessary part will be removed. next, the conductor exposed from the photosensitive resist — after etching a film part, all photosensitive resists exfoliate. in this way, the object for spiral-like coils — a conductor 33 and edge 33a are formed. The alignment mark 43 can be used also for the alignment at this time.

[0019] in this example, the alignment mark 43 is formed in two corners of the near side of a substrate 32 — having — the object for coils — a conductor 33 and the screening electrode 34 which has countered this align in all directions into each part surrounded with the alternate long and short dash line 45, and is arranged. and the alignment mark 43 — these objects for coils — it has position relation to the conductor 33 and the screening electrode 34.

[0020] On the other hand, the substrate 36 is also formed for the same for example, two or more screening-electrodes [with the means of photograph RISOGURAFU] 37, and two alignment mark 44 in the top face. The alignment mark 44 is formed in two corners by the side of the back of a substrate 36, and a screening electrode 37 aligns in all directions into each part surrounded with the alternate long and short dash line 46, and is arranged. And the alignment mark 44 has position relation to these screening electrodes 37. Furthermore, the notch 47 is formed in two corners of the near side of a substrate 36.

[0021] next, the substrate 32 — adhesives 8 — minding — a substrate 36 — joining — the object for coils — a conductor 33 is put. A substrate 32 and alignment between 36 are performed on the basis of the alignment marks 43 and 44, detecting, looking at the alignment marks 43 and 44 using one side alignment equipment 50, since the alignment mark 43 is exposed from the notch 47 at this time as shown in drawing 13 . it ** <TXF FR=0002 HE=250 WI=080 LX=1100 LY=0300> obtains and carries out, and as shown in drawing 14 , the inductor aggregate substrate 48 which consists of substrates 32 and 36 is obtained.

[0022] Next, looking at the alignment mark 43 (or 44), after setting the aggregate substrate 48 to the processing table of cutting equipment, the location of a processing table is adjusted detecting, the alignment mark 43 (or 44) is started, and it is made to move to a criteria location. Then, the aggregate substrate 48 is cut in all directions at the predetermined spacing on the basis of the alignment mark 43 (or 44) in cutting off wheel of cutting equipment (drawing 15 and 16 reference). In this way, the chip 49 cut into predetermined size is obtained. The external electrodes 40 and 41 are formed in the both ends of the obtained chip 49 by approaches, such as vacuum evaporationo and sputtering, or plating, spreading of conductive paste, etc., and it considers as the inductor 31 shown in drawing 10 .

[0023] In the manufacture approach of the above inductor 31, since the alignment mark 43 prepared in the substrate 32 was exposed from the notch 47, precision is improved by the alignment of substrates 32 and 36 on the basis of this alignment mark 43 and the alignment mark 44 prepared in the substrate 36. Therefore, precision is improved by junction of substrates 32 and 36. Moreover, alignment of substrates 32 and 36 can be carried out using cheap one

side alignment equipment, without being able to see the alignment marks 43 and 44 from the same, and using expensive double-sided alignment equipment. Furthermore, each chip 49 can be cut down with a sufficient precision on the basis of these alignment marks 43 and 44.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The sectional view showing the 1st example of the manufacture approach of the electronic parts concerning this invention.
[Drawing 2] The perspective view of the substrate used for the chip inductor shown in drawing 1 .
[Drawing 3] The sectional view for explaining the manufacture procedure of the 1st example.
[Drawing 4] The perspective view for explaining the manufacture procedure following drawing 3 .
[Drawing 5] The perspective view for explaining the manufacture procedure following drawing 4 .
[Drawing 6] The sectional view of the electronic-parts aggregate substrate shown in drawing 5 .
[Drawing 7] The perspective view for explaining the manufacture procedure following drawing 5 .
[Drawing 8] The perspective view for explaining the manufacture procedure following drawing 7 .
[Drawing 9] The sectional view of the electronic-parts aggregate substrate after the cut shown in drawing 8 .
[Drawing 10] The sectional view showing the 2nd example of the manufacture approach of the electronic parts concerning this invention.
[Drawing 11] The sectional view for explaining the manufacture procedure of the 2nd example.
[Drawing 12] The perspective view for explaining the manufacture procedure following drawing 11 .
[Drawing 13] The sectional view for explaining the manufacture procedure following drawing 12 .
[Drawing 14] The perspective view for explaining the manufacture procedure following drawing 13 .
[Drawing 15] The perspective view for explaining the manufacture procedure following drawing 14 .
[Drawing 16] The sectional view of the electronic-parts aggregate substrate after the cut shown in drawing 15 .
[Drawing 17] The perspective view showing other examples.
[Drawing 18] The perspective view showing other another examples.
[Drawing 19] The perspective view showing other still more nearly another examples.
[Description of Notations]
1 — Inductor
2 — Insulator substrate (the 1st substrate)
the object for 3 — coils — a conductor
6 — Insulator substrate (the 2nd substrate)
7 — Notch
15 — Alignment mark
18 — Inductor aggregate substrate
22 — Chip
31 — Inductor
32 — Insulator substrate (the 1st substrate)
the object for 33 — coils — a conductor
36 — Insulator substrate (the 2nd substrate)
37 — Screening electrode
43 — Alignment mark (the 1st alignment mark)
44 — Alignment mark (the 2nd alignment mark)
47 — Notch
48 — Inductor aggregate substrate
49 — Chip
54 — Insulator substrate (the 1st substrate)
55 — Insulator substrate (the 2nd substrate)
56 57 — Hole
60 — Insulator substrate (the 1st substrate)
61 — Insulator substrate (the 2nd substrate)
62 63 — Alignment mark
65 — Insulator substrate (the 1st substrate)
66 — Insulator substrate (the 2nd substrate)
67, 68, 69, 70 — Alignment mark

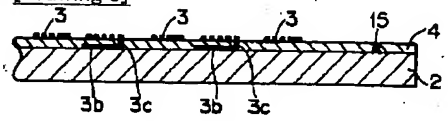
[Translation done.]

* NOTICES *

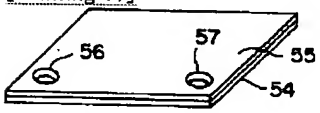
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

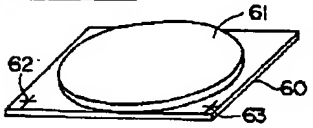
[Drawing 3]



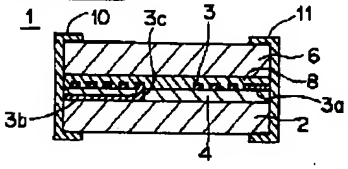
[Drawing 17]



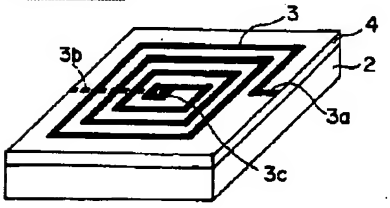
[Drawing 18]



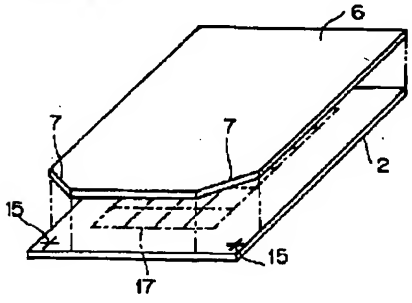
[Drawing 1]



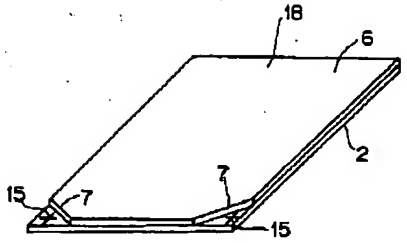
[Drawing 2]



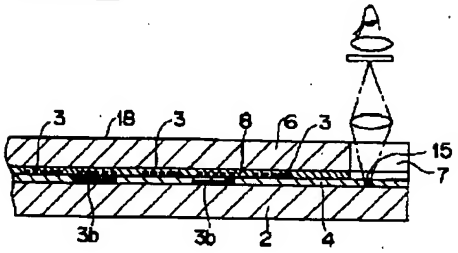
[Drawing 4]



[Drawing 5]



[Drawing 6]



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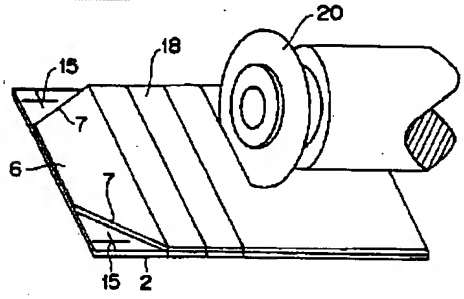

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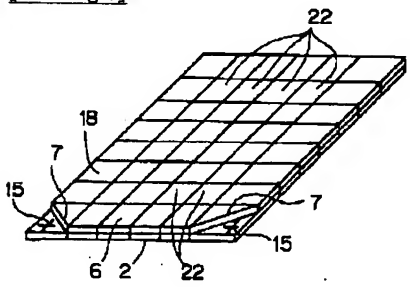

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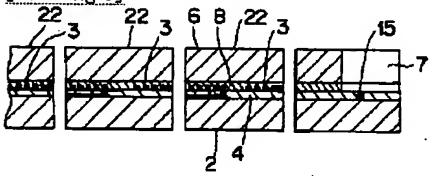
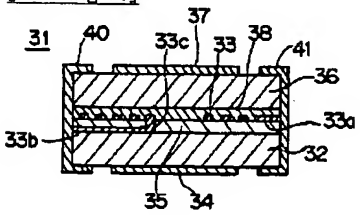
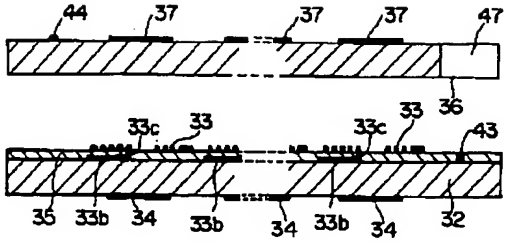


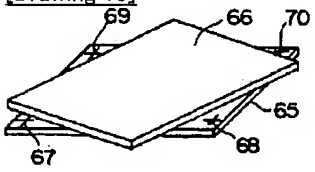
[Drawing 10]



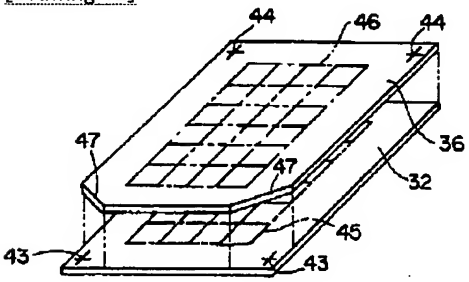
[Drawing 11]



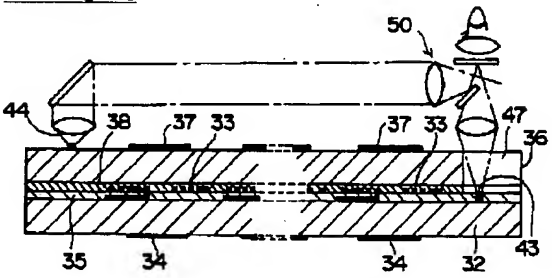
[Drawing 19]



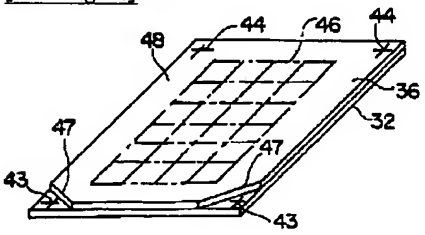
[Drawing 12]



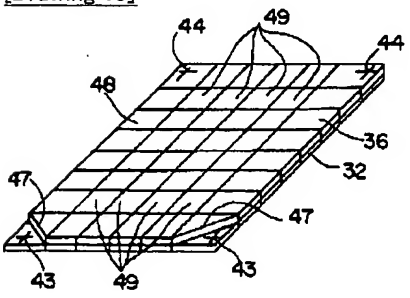
[Drawing 13]



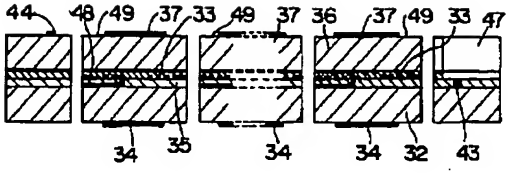
[Drawing 14]



[Drawing 15]



[Drawing 16]



[Translation done.]

GP-448-3 (NP-1480)

(1.)

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平7－263268

(43)公開日　平成７年(1995)10月13日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｆ　41/04	Ｂ			
Ｈ０５Ｋ　1/14	Ａ			

審査請求　未請求　請求項の数２　ＯＬ　（全７頁）

(21)出願番号　特願平6－46620

(22)出願日　平成６年(1994)３月17日

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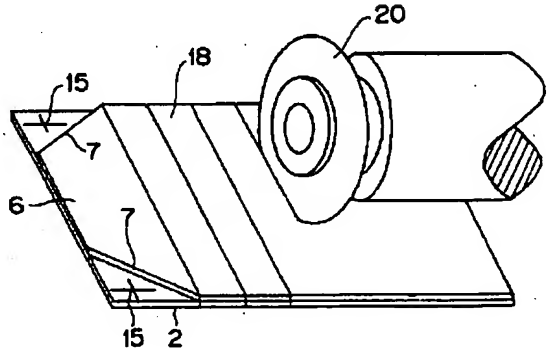
(54)【発明の名称】　電子部品の製造方法

(57)【要約】

【目的】　高価な装置を使用しなくても、安価な製造コストで基板相互を精度良く位置合わせして接合し、電子部品集合体基板から電子部品チップを精度良く切り出す。

【構成】　コイル用導体とアライメントマーク１５を同一面に設けた絶縁体基板２と、アライメントマーク１５を露出させるための切欠き７を設けた絶縁体基板６を接合して、インダクタ集合体基板１８を構成する。コイル用導体とアライメントマーク１５は所定の位置関係を有するように設定されている。切欠き７から露出したアライメントマーク１５を基準にして切削装置の切断砥石２０にて集合体基板１８をカットし、チップを切り出す。



【特許請求の範囲】
【請求項１】　第１基板の一面に、パターン導体とこのパターン導体に対して所定の位置関係を有するアライメントマークとを設ける工程と、
前記アライメントマークが露出し、かつ前記パターン導体を挟むように、前記第１基板と第２基板とを接合し、電子部品集合体基板を構成する工程と、
露出した前記アライメントマークを基準にして前記電子部品集合体基板から所定サイズの電子部品チップを切り出す工程と、
を備えたことを特徴とする電子部品の製造方法。
【請求項２】　第１基板の一面に、第１パターン導体とこの第１パターン導体に対して所定の位置関係を有する第１アライメントマークとを設ける工程と、
第２基板の一面に、第２パターン導体とこの第２パターン導体に対して所定の位置関係を有する第２アライメントマークとを設ける工程と、
前記第２パターン導体と第２アライメントマークを外側にした状態で、前記第１のアライメントマークが露出し、かつ前記第１パターン導体を挟むように、前記第１基板と第２基板を重ねた後、前記第１アライメントマークと前記第２アライメントマークを基準にし前記第１基板と第２基板相互の位置合わせをする工程と、
前記第１基板に前記第２基板を接合して電子部品集合体基板を構成する工程と、
前記電子部品集合体基板から所定サイズの電子部品チップを切り出す工程と、
を備えたことを特徴とする電子部品の製造方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、内部にパターン導体を備えた電子部品の製造方法に関する。
【０００２】
【従来の技術と課題】複数の基板を接合して構成される電子部品の製造方法において、従来より基板縁端を基準にして基板相互の位置合わせをして接合する方法が知られていた。また、基板縁端を基準にして電子部品集合体基板から所定サイズの電子部品チップを切り出す方法も知られていた。しかしながら、これらの方法は基板縁端を高精度に仕上げることが難しいため、位置合わせ精度や切り出し精度が低いという問題があった。
【０００３】また、別の方法として、基板にアライメントマークを設け、このアライメントマークを基準にして基板相互の位置合わせを行なう方法がある。また、アライメントマークを基準にして電子部品集合体基板から所定サイズの電子部品チップを切り出す方法もある。これらの方法は、基板縁端を基準にする方法よりも精度が高くなるが、アライメントマークを接合面以外の面に設ける必要がある。なぜなら、接合面にアライメントマークを設けると、基板を接合した後はアライメントマークが基板に挟み込まれて見えなくなり基準として利用できなくなるからである。従って、製造工数が増加したり、アライメントマークが基板の表裏に設けられている場合には高価な両面位置合わせ装置が特別に必要である等の問題が新たに発生する。
【０００４】そこで、本発明の課題は、高価な装置を使用しなくても、安価な製造コストで基板相互を精度良く位置合わせして接合することができ、電子部品集合体基板から電子部品チップを精度良く切り出すことができる電子部品の製造方法を提供することにある。
【０００５】
【課題を解決するための手段と作用】以上の課題を解決するため、本発明に係る電子部品の製造方法は、（ａ）第１基板の一面に、パターン導体とこのパターン導体に対して所定の位置関係を有するアライメントマークとを設ける工程と、（ｂ）前記アライメントマークが露出し、かつ前記パターン導体を挟むように、前記第１基板と第２基板とを接合し、電子部品集合体基板を構成する工程と、（ｃ）露出した前記アライメントマークを基準にして前記電子部品集合体基板から所定サイズの電子部品チップを切り出す工程と、を備えたことを特徴とする。
【０００６】以上の方法において、第１基板に設けたアライメントマークが露出しているため、従来のようにアライメントマークを接合面以外の面に設ける必要がなくなり、製造工数が減少する。そして、電子部品集合体基板からの電子部品チップの切り出しは、アライメントマークを基準にして行われるため、切り出し精度が高くなる。
【０００７】また、本発明に係る電子部品の製造方法は、（ｄ）第１基板の一面に、第１パターン導体とこの第１パターン導体に対して所定の位置関係を有する第１アライメントマークとを設ける工程と、（ｅ）第２基板の一面に、第２パターン導体とこの第２パターン導体に対して所定の位置関係を有する第２アライメントマークとを設ける工程と、（ｆ）前記第２パターン導体と第２アライメントマークを外側にした状態で、前記第１のアライメントマークが露出し、かつ前記第１パターン導体を挟むように、前記第１基板と第２基板を重ねた後、前記第１アライメントマークと前記第２アライメントマークを基準にし前記第１基板と第２基板相互の位置合わせをする工程と、（ｇ）前記第１基板に前記第２基板を接合して電子部品集合体基板を構成する工程と、（ｈ）前記電子部品集合体基板から所定サイズの電子部品チップを切り出す工程と、を備えたことを特徴とする。
【０００８】以上の方法において、第１アライメントマークと第２アライメントマークを同一方向から見ることができるため、安価な片面位置合わせ装置を用いて第１基板と第２基板の位置合わせが精度良く行なわれる。
【０００９】

【実施例】以下、本発明に係る電子部品の製造方法の実施例について添付図面を参照して説明する。

［第１実施例、図１～図９］第１実施例は、図１に示すインダクタ１の製造方法について説明する。

【００１０】インダクタ１は、コイル用導体３を上面に設けた絶縁体基板２と、表面に何も設けない絶縁体基板６とを、接着剤８にて接合したものである。基板２，６の材料としては、例えばフェライト等が用いられる。基板２は、図２に示すように、上面に絶縁膜（例えばポリイミド膜）４を介して渦巻状コイル用導体３が設けられている。コイル用導体３の一方の端部３ａは基板２の右側縁部に露出し、他方の端部３ｂは絶縁膜４に設けたスルーホール３ｃを介して基板２の中央部から左側縁部に引き回されている。

【００１１】インダクタ１の左右の端部にはそれぞれ外部電極１０，１１が設けられている。コイル用導体３の端部３ｂは外部電極１０に電気的に接続され、端部３ａは外部電極１１に電気的に接続されている。次に、以上の構造を有するインダクタ１の製造手順について説明する。通常、チップ部品の量産においては、複数のチップ部品を含む集合体基板の状態で製造される。インダクタ１も同様に、図３及び図４に示すように、基板２に複数のコイル用導体３と、それらの導体、絶縁層パターンの相互の位置関係を規制するためのアライメントマーク１５が設けられる。すなわち、基板２の上面に、まず全面に蒸着、スパッタリング、めっき他の手段により導体膜が形成される。次に、感光性レジストを塗布した後、露光機により所定のパターンが焼き付けられ、現像されると、不要な部分の感光性レジストが除去される。次に、感光性レジストから露出している導体膜部分をエッチングした後、感光性レジストは全て剥離する。こうしてコイル用導体３の端部３ｂと、アライメントマーク１５のパターンに相当する導体のパターンが形成される。次に、基板全面に例えば紫外線硬化性のポリイミド樹脂もしくはその前駆物質を塗布し、露光、現像、硬化により端部３ｂの形成部分を残した絶縁膜を形成する。このときのパターン合わせには、フォトマスクに適当なアライメントマークを設置して、アライメントマーク１５と合致させることができる。次に、同様のパターン形成手段により、スパイラル状のコイル用導体３と端部３ａの形成がされる。このときの位置合わせにもアライメントマーク１５は使用できる。なお、導体、絶縁膜のパターン形成は、前記薄膜工法によらず、選択めっきやスクリーン印刷他の厚膜工法によるものであってもよい。

【００１２】アライメントマーク１５は基板２の手前側の少なくとも二つの隅部に設けられ、コイル用導体３は一点鎖線１７にて囲まれた部分に縦横に整列して配置されている。そして、アライメントマーク１５はこれらのコイル用導体３に対して所定の位置関係を有している。この基板２に、表面に何も設けない基板６を接着剤８を介して接合し、基板２と基板６にてコイル用導体３を挟み込む。基板６の手前側の二つの隅部には切欠き７が設けられており、基板２と基板６の接合後も、切欠き７からアライメントマーク１５が露出している（図５参照）。こうして、基板２と基板６からなるインダクタ集合体基板１８が得られる。

【００１３】次に、集合体基板１８を切削装置の加工テーブルにセットした後、図６に示すように、アライメントマーク１５を見ながら（検出しながら）加工テーブルの位置を調整し、アライメントマーク１５を切り出し基準位置に移動させる。この後、図７に示すように、切削装置の切断砥石２０にてアライメントマーク１５を基準にして所定の間隔で集合体基板１８を縦横にカットする。こうして、所定サイズにカットされたチップ２２が得られる（図８及び図９参照）。得られたチップ２２の両端部に、蒸着、スパッタリング等の方法、もしくはめっき、導電ペーストの塗布等により外部電極１０，１１を形成し、図１に示したインダクタ１とする。

【００１４】以上のインダクタ１の製造方法において、アライメントマーク１５を切欠き７から露出させたため、このアライメントマーク１５を基準にして各チップ２２の切り出し位置を精度良く確定することができる。従って、チップ２２を精度良く切り出すことができる。また、アライメントマーク１５を基板２の接合面、すなわちコイル用導体３が設けられている面に設ければよいので、従来のようにアライメントマークを接合面以外の面（本実施例の場合は基板２の下面）に特別に設ける必要がなくなる。この結果、基板２下面のパターン形成工程が省略でき、安価な両面位置合わせ装置も不要となり、製造コストを下げることができる。

【００１５】［第２実施例、図１０～図１６］第２実施例は、図１０に示すインダクタ３１の製造方法について説明する。インダクタ３１は、コイル用導体３３とシールド電極３４をそれぞれ上下面に設けた絶縁体基板３２と、上面にシールド電極３７を設けた絶縁体基板３６とを、接着剤３８にて接合したものである。

【００１６】絶縁体基板３２は、上面に絶縁膜（例えばポリイミド膜）３５を介して渦巻状コイル用導体３３が設けられている。コイル用導体３３の一方の端部３３ａは、インダクタ３１の右端部に設けられた外部電極４１に電気的に接続されている。コイル用導体３３の他方の端部３３ｂは、絶縁膜３５に設けられたスルーホール３３ｃを介してインダクタ３１の中央部から左側に引き回され、インダクタ３１の左端部に設けられた外部電極４０に電気的に接続されている。

【００１７】次に、以上の構造を有するインダクタ３１の製造手順について説明する。図１１及び図１２に示すように、基板３２に例えばフォトリソグラフの手段にて複数のコイル用導体３３及びシールド電極３４と二つ以上のアラインメントマーク４３が設けられる。すなわ

ち、基板３２の上下面に、蒸着、スパッタリング、めっき他の手段により導体膜を形成する。次に、感光性レジストを基板３２の上下全面に塗布した後、基板３２を両面露光機にセットする。このとき、基板３２は、１対１に対応させた２枚のフォトマスクの間に挟み込まれる。そして、基板３２の上下面を同時に露光した後、感光性レジストが現像され、不要な部分の感光性レジストが除去される。次に、感光性レジストから露出している薄膜部分をエッチングした後、残っている感光性レジストを全て剥す。こうして、コイル用導体３３の端部３３ｂとアライメントマーク４３とシールド電極３４を形成する。

【００１８】次に、基板３２の全面に例えば紫外線硬化性のポリイミド樹脂もしくはその前駆物質を塗布し、露光、現像、硬化により端部３３ｂの形成部分を残した絶縁膜３５を形成する。このときのパターン合わせには、フォトマスクに適当なアライメントマークを設置して、アライメントマーク４３と合致させることができる。次に、基板３２の上面全面に蒸着、スパッタリング、めっき他の手段により導体膜が形成される。次に、感光性レジストを塗布した後、露光機により所定のパターンが焼き付けられ、現像されると、不要な部分の感光性レジストが除去される。次に、感光性レジストから露出している導体膜部分をエッチングした後、感光性レジストは全て剥離する。こうしてスパイラル状のコイル用導体３３と端部３３ａが形成される。このときの位置合わせにも、アライメントマーク４３を使用することができる。

【００１９】この例では、アライメントマーク４３は基板３２の手前側の二つの隅部に設けられ、コイル用導体３３とこれに対向しているシールド電極３４は一点鎖線４５にて囲まれた各部分に縦横に整列して配置されている。そして、アライメントマーク４３はこれらのコイル用導体３３及びシールド電極３４に対して所定の位置関係を有している。

【００２０】一方、基板３６も、同様に例えばフォトリソグラフの手段にて複数のシールド電極３７と二つのアライメントマーク４４がその上面に設けられている。アライメントマーク４４は基板３６の奥側の二つの隅部に設けられ、シールド電極３７は一点鎖線４６にて囲まれた各部分に縦横に整列して配置されている。そして、アライメントマーク４４はこれらのシールド電極３７に対して所定の位置関係を有している。さらに、基板３６の手前側の二つの隅部には切欠き４７が設けられている。

【００２１】次に、基板３２に、接着剤８を介して基板３６を接合し、コイル用導体３３を挟み込む。このとき、図１３に示すように、アライメントマーク４３は切欠き４７から露出しているので、アライメントマーク４３と４４を片面位置合わせ装置５０を使用して見ながら（検出しながら）、アライメントマーク４３，４４を基準にして基板３２と３６相互の位置合わせを行なう。こうして、図１４に示すように、基板３２と３６からなるインダクタ集合体基板４８が得られる。

【００２２】次に、集合体基板４８を切削装置の加工テーブルにセットした後、アライメントマーク４３（あるいは４４）を見ながら（検出しながら）、加工テーブルの位置を調整し、アライメントマーク４３（あるいは４４）を切り出し基準位置に移動させる。この後、切削装置の切断砥石にてアライメントマーク４３（あるいは４４）を基準にして所定の間隔で集合体基板４８を縦横にカットする（図１５及び１６参照）。こうして所定サイズにカットされたチップ４９が得られる。得られたチップ４９の両端部に、蒸着、スパッタリング等の方法、もしくはめっき、導電ペーストの塗布等により外部電極４０，４１を形成し、図１０に示したインダクタ３１とする。

【００２３】以上のインダクタ３１の製造方法において、基板３２に設けたアライメントマーク４３を切欠き４７から露出させたため、このアライメントマーク４３と基板３６に設けたアライメントマーク４４を基準にして基板３２と３６の位置合わせが精度良くできる。従って、基板３２と３６の接合が精度良くできる。また、アライメントマーク４３と４４を同一方向から見ることができ、高価な両面位置合わせ装置を使用することなく、安価な片面位置合わせ装置を用いて基板３２と３６の位置合わせをすることができる。さらに、このアライメントマーク４３，４４を基準にして各チップ４９を精度良く切り出すことができる。

【００２４】［他の実施例］本発明に係る電子部品の製造方法は前記実施例に限定するものではなく、その要旨の範囲内で種々に変形することができる。前記実施例においては、アライメントマークを露出させるために切欠きを設けたが、必らずしも切欠きを設ける必要はないし、またアライメントマークの数も２個に限る必要もない。例えば、図１７に示すように、穴５６，５７を設けた絶縁体基板５５を、回路導体とアライメントマークを設けた絶縁体基板５４に接合し、穴５６，５７からアライメントマークが露出するようにしてもよい。また、図１８に示すように、円形絶縁体基板６１を、回路導体とアライメントマーク６２，６３を設けた絶縁体基板６０に接合してアライメントマーク６２，６３が露出するようにしてもよい。また、図１９に示すように、矩形絶縁体基板６６を、回路導体と４個のアライメントマーク６７，６８，６９，７０を設けた絶縁体基板６５に接合してアライメントマーク６７～７０が露出するようにしてもよい。

【００２５】さらに、アライメントマークは、前記実施例のように回路導体と共に同時期に形成してもよいし、回路導体形成時とは別時期に独立して形成してもよい。ただし、回路導体とアライメントマークを同時期に形成すれば、位置合わせ精度や切り出し精度がより向上する

と共に、製造工数も少なくなる。また、回路導体はコイル用導体に限ることなく、電気的機能をもつものであれば形状、材質等を問わない。

【００２６】

【発明の効果】以上の説明で明らかなように、本発明によれば、第１基板に設けたアラインメントマークが露出しているので、このアライメントマークを基準にして、電子部品集合体基板からの電子部品チップの切り出しを精度良く行なうことができる。また、アライメントマークをパターン導体と同一面に設ければよいので、従来のようにアライメントマークを接合面以外の面に設ける必要がなくなり、製造工数を少なくすることができる。

【００２７】また、第１基板に設けた第１アライメントマークが露出しているので、第１アライメントマークと第２アライメントマークを基準にして第１基板と第２基板の位置合わせが精度良くできる。さらに、第１アライメントマークと第２アライメントマークを同一方向から見ることができるので、高価な両面位置合わせ装置を使用することなく、安価な片面位置合わせ装置を用いて第１基板と第２基板の位置合わせをすることができる。

【００２８】この結果、高価な装置を使用しなくても、安価な製造コストで基板相互を精度良く位置合わせして接合することができ、電子部品集合体基板から電子部品チップを精度良く切り出すことができる

【図面の簡単な説明】

【図１】本発明に係る電子部品の製造方法の第１実施例を示す断面図。

【図２】図１に示したチップインダクタに用いられる基板の斜視図。

【図３】第１実施例の製造手順を説明するための断面図。

【図４】図３に続く製造手順を説明するための斜視図。

【図５】図４に続く製造手順を説明するための斜視図。

【図６】図５に示した電子部品集合体基板の断面図。

【図７】図５に続く製造手順を説明するための斜視図。

【図８】図７に続く製造手順を説明するための斜視図。

【図９】図８に示したカット後の電子部品集合体基板の断面図。

【図１０】本発明に係る電子部品の製造方法の第２実施例を示す断面図。

【図１１】第２実施例の製造手順を説明するための断面図。

【図１２】図１１に続く製造手順を説明するための斜視図。

【図１３】図１２に続く製造手順を説明するための断面図。

【図１４】図１３に続く製造手順を説明するための斜視図。

【図１５】図１４に続く製造手順を説明するための斜視図。

【図１６】図１５に示したカット後の電子部品集合体基板の断面図。

【図１７】他の実施例を示す斜視図。

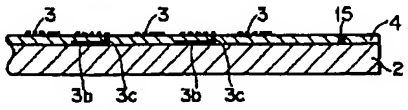
【図１８】別の他の実施例を示す斜視図。

【図１９】さらに別の他の実施例を示す斜視図。

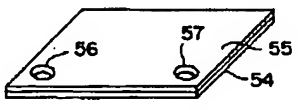
【符号の説明】

１…インダクタ
２…絶縁体基板（第１基板）
３…コイル用導体
６…絶縁体基板（第２基板）
７…切欠き
１５…アラインメントマーク
１８…インダクタ集合体基板
２２…チップ
３１…インダクタ
３２…絶縁体基板（第１基板）
３３…コイル用導体
３６…絶縁体基板（第２基板）
３７…シールド電極
４３…アライメントマーク（第１アライメントマーク）
４４…アライメントマーク（第２アライメントマーク）
４７…切欠き
４８…インダクタ集合体基板
４９…チップ
５４…絶縁体基板（第１基板）
５５…絶縁体基板（第２基板）
５６，５７…穴
６０…絶縁体基板（第１基板）
６１…絶縁体基板（第２基板）
６２，６３…アライメントマーク
６５…絶縁体基板（第１基板）
６６…絶縁体基板（第２基板）
６７，６８，６９，７０…アライメントマーク

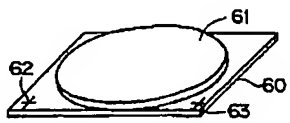
【図３】



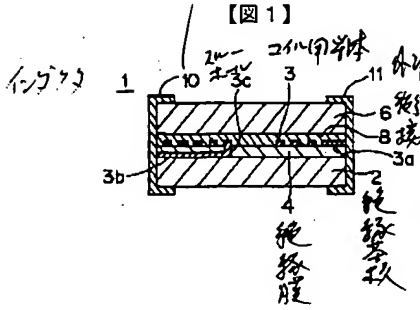
【図１７】



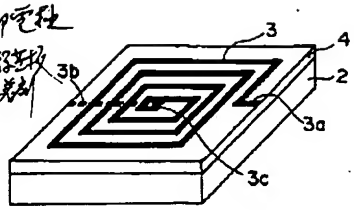
【図１８】



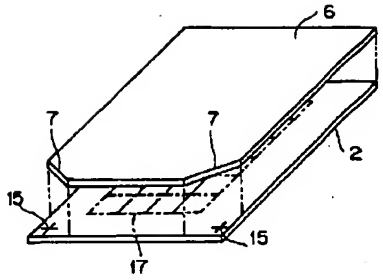
【図１】



【図２】



【図４】



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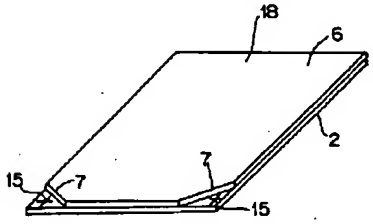

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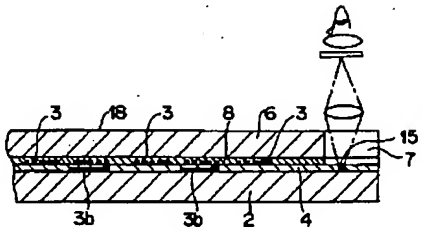

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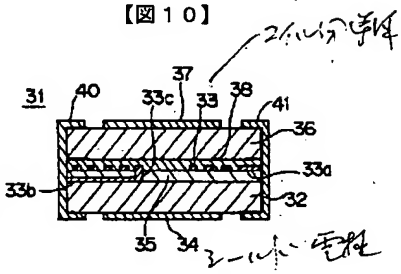

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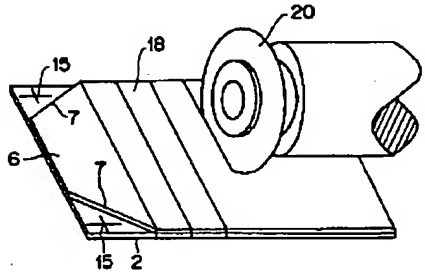

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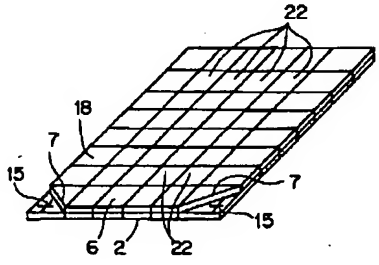

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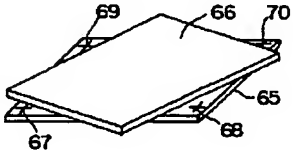

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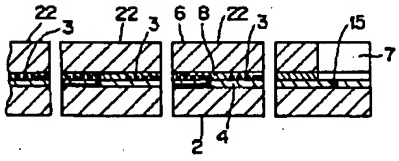

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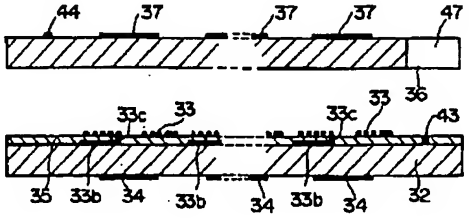

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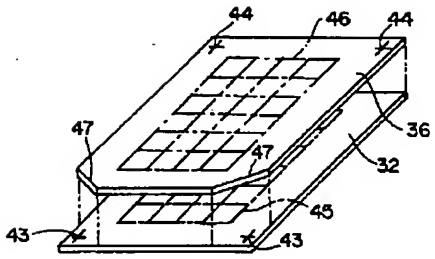

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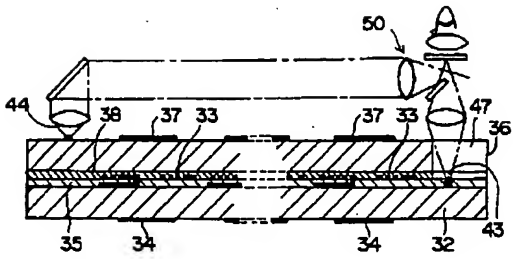

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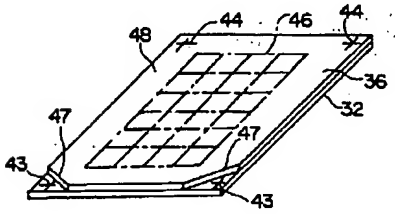

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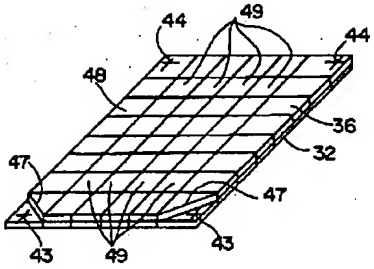

【図１６】